METHOD FOR READING MEMORY CELLS

The Field of the Invention

[0001] The present invention generally relates to magnetic memory cells. More particularly, the present invention relates to a method for reading the magnetization orientation of such devices.

Background of the Invention

[0002] Magnetic random access memory (MRAM) is a non-volatile thin-film memory that is used for data storage. A typical MRAM device includes an array of memory cells. Conductive traces (commonly referred to as word lines and bit lines) are routed across the array of memory cells. Word lines extend along rows of the memory cells, and bit lines extend along columns of the memory cells. Each memory cell is located at a cross point of a word line and a bit line, and stores a single bit of information.

[0003] The memory cells may be magnetic memory cells, such as spin dependent tunneling junctions. A typical magnetic memory cell includes a layer of ferromagnetic film in which the magnetization orientation is alterable (referred to as a sense layer or a data storage layer), and a layer of ferromagnetic film in which the magnetization orientation is fixed in a particular direction (referred to as a reference layer or a pinned layer). An insulating tunnel barrier is sandwiched between the ferromagnetic layers.

[0004] A logic value may be written to a magnetic memory cell by applying a magnetic field that sets the relative orientations of the memory cell's sense layer and reference layer to either parallel (logic "0") or anti-parallel (logic "1"). The magnetization orientation in the sense layer aligns along an axis of the sense layer that is commonly referred to as its easy axis. External magnetic fields are applied to flip the magnetization orientation in the sense layer along its easy axis to either a parallel or anti-parallel orientation with respect to the magnetization orientation of the reference layer, depending on the desired logic state. The magnetization orientation of each memory cell will thus assume one of two

stable orientations at any given time (i.e., parallel or anti-parallel). The parallel or anti-parallel orientation of the memory cell's ferromagnetic layers determines the resistance state of the memory cell, with a parallel orientation corresponding to a low resistance state, and an anti-parallel orientation corresponding to a high resistance state.

[0005] The external magnetic fields used to flip the magnetization orientation of the sense layer in a selected memory cell are created by supplying current to the word line and the bit line crossing the selected memory cell. The currents in the word line and bit line create magnetic fields that, when combined, can switch the magnetization orientation of the selected memory cell from parallel to anti-parallel or vice versa. Other unselected memory cells receive only a single magnetic field from either the word line or the bit line crossing the unselected memory cells. The magnitudes of the magnetic fields are chosen to be low enough so that the unselected memory cells do not switch their magnetization orientations when subjected to a single magnetic field from either the word line or the bit lines. An undesired switching of a memory cell that is subject only to the word line magnetic field or the write line magnetic field is commonly referred to as half-select switching.

[0006] As noted above, the logic value stored in a magnetic memory cell is determined by the parallel or anti-parallel orientation of the memory cell. Also, the parallel or anti-parallel orientation of the memory cell determines the resistance state of the memory cell. Thus, the logic value stored in the memory cell may be read by sensing the resistance state of the memory cell. However, the absolute difference between the resistance of a memory cell having a parallel orientation and the resistance of a memory cell having an anti-parallel orientation may be very small. Therefore, the act of measuring the resistance (i.e., reading the data in the memory cell) can itself introduce some uncertainty into the accuracy of the measurement. The act of measuring the resistance may also alter the magnetization orientation of the memory cell. If the magnetization orientation of the memory cell is altered (i.e., the reading operation is

destructive), the data must also be written back into the memory cell after the data is read.

Summary of the Invention

[0007] The present invention provides a method for reading the magnetization orientation of a memory cell. In one embodiment according to the invention, the method comprises applying a magnetic field to the memory cell, observing any change in resistance of the memory cell as the magnetic field is applied, and determining the magnetization orientation based upon the observed change in resistance of the memory cell.

Brief Description of the Drawings

[0008] Embodiments of the invention are better understood with reference to the following drawings. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

[0009] Figures 1a and 1b are top and profile views of a prior art MRAM array.

[0010] Figures 2a through 2c are profile and side views of a prior art MRAM memory cell illustrating an orientation of magnetization of active and reference magnetic films.

[0011] Figure 3 is a profile view of a prior art memory cell, its write lines, and magnetic fields generated by currents flowing through the write lines.

[0012] Figure 4 is an example of a hysteresis loop showing resistance versus applied magnetic field in a memory cell whose magnetization orientation can be read according to embodiments of the invention.

[0013] Figure 5 is an illustration of magnetic fields in a memory cell whose magnetization orientation can be read according to embodiments of the invention, the memory cell displaying a parallel magnetization orientation.

[0014] Figures 6a-6c are illustrations of magnetic fields in the sense layer of a memory cell whose magnetization orientation can be read according to embodiments of the invention, the illustrated magnetization orientation moving

progressively from a parallel orientation toward an anti-parallel orientation as the magnetic field strength increases toward a critical value.

[0015] Figure 7 is an illustration of magnetic fields in a memory cell whose magnetization orientation can be read according to embodiments of the invention, the memory cell displaying an anti-parallel magnetization orientation.

[0016] Figures 8a-8c are illustrations of magnetic fields in the sense layer of a memory cell whose magnetization orientation can be read according to embodiments of the invention, the illustrated magnetization orientation remaining unmoved from an anti-parallel orientation toward a parallel orientation at magnetic strengths less than a critical value.

[0017] Figure 9a illustrates $\delta R/\delta H$ of the hysteresis loop of Figure 4, as the magnetization orientation of the memory cell changes from anti-parallel to parallel, which is used by embodiments of the invention for reading the magnetization orientation of the memory cell.

[0018] Figure 9b illustrates $\delta R/\delta H$ of the hysteresis loop of Figure 4, as the magnetization orientation of the memory cell changes from parallel to anti-parallel, which is used by embodiments of the invention for reading the magnetization orientation of the memory cell.

[0019] Figures 10a-10d are exemplary shapes of a memory cell sense layer which enhance the edge domain effect in a memory cell whose magnetization orientation can be read according to embodiments of the invention.

[0020] Figure 11 is a block diagram illustrating one embodiment of a system for implementing the various embodiments for reading the magnetization orientation of a memory cell according to the invention.

Detailed Description

[0021] Figure 1 illustrates a top plan view of a simplified prior art MRAM array 100. The array 100 includes memory cells 120, word lines 130, and bit lines 132. The memory cells 120 are positioned at each intersection of a word line 130 with a bit line 132. Most commonly, the word lines 130 and bit lines 132 are arranged in orthogonal relation to one another. The memory cells 120 are positioned between the word and bit lines 130,132, as illustrated in Figure 1b.

For example, the bit lines 132 can be positioned above the memory cells 120 and the word lines 130 can be positioned below. Because the word lines and the bit lines operate in combination to switch the magnetization orientation of the selected memory cell (i.e., to write the memory cell), the word lines and bit lines can be collectively referred to as write lines.

[0022] Figures 2a through 2c illustrate the storage of a bit of data in a single memory cell 120. In Figure 2a, the memory cell 120 includes a sense layer 122 and a reference layer 124 which are separated by a dielectric region 126. The magnetization orientation in the sense layer 122 is not fixed and can assume either of two stable orientations as shown by arrow M_1. On the other hand, the reference layer 124 has a fixed magnetization orientation shown by arrow M_2. The sense layer 122 rotates its magnetization orientation in response to electrical currents applied to the write lines (130,132, not shown) during a write operation to the memory cell 120. The first logic state of the data bit stored in memory cell 120 is indicated when M_1 and M_2 are parallel to each other as illustrated in Figure 2b. For instance, when M_1 and M_2 are parallel a logic "0" state is stored in the memory cell 120. Conversely, a second logic state is indicated when M_1 and M_2 are anti-parallel to each other as illustrated in Figure 2c. Similarly, when M_1 and M_2 are anti-parallel a logic "1" state is stored in the memory cell 120. In Figures 2b and 2c the dielectric region 126 has been omitted. Although Figures 2a through 2c illustrate the sense layer 122 positioned above the reference layer 124, the reference layer 124 can be positioned above the sense layer 122.

[0023] The resistance of the memory cell 120 differs according to the relative orientations of M_1 and M_2. When M_1 and M_2 are anti-parallel, i.e., the logic "1" state, the resistance of the memory cell 120 is at its highest. On the other hand, the resistance of the memory cell 120 is at its lowest when the orientations of M_1 and M_2 are parallel, i.e., the logic "0" state. As a consequence, the logic state of the data bit stored in the memory cell 120 can be determined by measuring its resistance. The resistance of the memory cell 120 is reflected by a magnitude of a sense current 123 (referring to Figure 2a) that flows in response to read voltages applied to the word and bit lines 130,132.

[0024] In Figure 3, the memory cell 120 is positioned between the write lines 130,132. The separate sense and reference layers 122, 124 are not shown in Figure 3. The magnetization orientation of the memory cell 120 is altered in response to a current I_x that generates a magnetic field H_y and a current I_y that generates a magnetic field H_x. The magnetic fields H_x and H_y act in combination to rotate the magnetization orientation of the memory cell 120.

[0025] As can be seen from Figure 4, as the magnetization orientation of the memory cell 120 changes from one magnetization orientation to another (i.e., parallel to anti-parallel or anti-parallel to parallel), a plot of the memory cell resistance R versus the applied magnetic field H follows a hysteresis loop 200. The shape of the resistance R versus magnetic field Hx plot is different, depending on whether the memory cell 120 is going from low resistance (parallel state) to high resistance (anti-parallel state), or from high resistance to low resistance. Specifically, the change from a high resistance to a low resistance is more abrupt than the change from a low resistance to a high resistance. This shape difference of the hysteresis loop 200 may be exploited to read the data in the memory cell 120 with a high degree of accuracy, without altering the resistance state (and thus the data) stored in the memory cell 120.

[0026] The reason for the shape of the hysteresis loop 200 can be better understood by examining the magnetization orientations of the sense layer 122 and reference layer 124 in memory cell 120 as the memory cell orientation switches from parallel (low resistance) to anti-parallel (high resistance) and from anti-parallel to parallel. In Figure 5, a parallel magnetization orientation of M_1 in sense layer 122 and M_2 in reference layer 124 is illustrated. For purposes of explanation and clarity, in Figure 5 top views of sense layer 122 and reference layer 124 are illustrated side-by-side and separately, although in actuality they would be stacked on top of each other. As illustrated in Figure 5, in a parallel state, sense layer 122 and reference layer 124 both have similar net charges on the same sides of the layers (e.g., a net negative charge on the left hand side and a net positive charge on the right hand side).

[0027] In a parallel magnetization orientation state of memory cell 120, as shown in Figure 5, the net magnetic charges of sense layer 122 and reference layer 124 force the formation of edge domains 210 in sense layer 122. As a negative magnetic field Hx (i.e. a field forcing the magnetic field M_1 of sense layer 122 to an anti-parallel orientation) is applied to sense layer 122, the edge domains 210 slowly grow until negative magnetic field Hx reaches a critical strength and the magnetization orientation of M_1 in sense layer 122 abruptly switches direction to an anti-parallel state. This effect is illustrated in Figures 6a-6c, in which only sense layer 122 is shown. In Figure 6a, the applied magnetic field Hx is 0. In Figure 6b, the applied magnetic field Hx is -0.25Hc, where Hc is the critical magnetic field that will cause the magnetization orientation of M_1 in sense layer 122 to switch direction to an anti-parallel state. In Figure 6c, the applied magnetic field Hx is -0.50Hc. As the magnitude of the applied magnetic field Hx grows toward the critical magnetic field Hc, edge domains 210 continue to grow toward the center of sense layer 122, until total reversal of the magnetization orientation of M_1 in sense layer 122 occurs. As illustrated by portion 202 of hysteresis loop 200 in Figure 4, the parallel to anti-parallel reversal of the magnetization orientation of M_1 in sense layer 122 may be characterized by a gradual and then increasingly rapid change from low resistance to high resistance as the magnitude of the negative magnetic field is increased. After the magnitude of the applied magnetic field Hx surpasses the critical magnetic field Hc, any further increase in the magnitude of the magnetic field has no effect on the resistance R.

[0028] For comparison, in Figure 7 an anti-parallel magnetization orientation of M_1 in sense layer 122 and M_2 in reference layer 124 is illustrated. For purposes of explanation and clarity, in Figure 7 top views of sense layer 122 and reference layer 124 are illustrated side-by-side and separately, although in actuality they would be stacked on top of each other. As illustrated in Figure 7, in an anti-parallel state, sense layer 122 and reference layer 124 have different net charges on the sides of the layers (e.g., reference layer 124 has a net negative charge on its left hand side and a net positive charge on its right hand side, while sense

layer 122 has a net positive charge on its left hand side and a net negative charge on its right hand side).

[0029] In an anti-parallel magnetization orientation state of memory cell 120, as shown in Figure 7, the net magnetic charges of sense layer 122 and reference layer 124 effectively cancel each other and no edge domains are formed in sense layer 122. As a positive magnetic field Hx (i.e. a field forcing the magnetic field of sense layer to a parallel orientation) is applied to sense layer 122, no effect is seen in the magnetic orientation of M_1 in sense layer 122. Only when magnetic field Hx reaches a critical strength Hc will the magnetization orientation of M_1 in sense layer 122 abruptly switches direction to a parallel state. This effect is illustrated in Figures 8a-8c, in which only sense layer 122 is shown. In Figure 8a, the applied magnetic field Hx is 0. In Figure 8b, the applied magnetic field Hx is 0.25Hc, where Hc is the critical magnetic field that will cause the magnetization orientation of M_1 in sense layer 122 to switch direction to a parallel state. In Figure 8c, the applied magnetic field Hx is 0.50Hc. In contrast to the gradual parallel to anti-parallel switch illustrated in Figures 6a-6c, in the anti-parallel to parallel switch illustrated in Figures 8a-8c as the applied magnetic field Hx grows toward the critical magnetic field Hc, no effect is seen in the magnetization orientation of M_1 in sense layer 122 (or in the resistance of memory cell 120) until magnetic field Hx reaches a critical strength Hc. When the magnetic field reaches the critical strength Hc, the magnetization orientation of M_1 in sense layer 122 abruptly switches direction to a parallel state. As illustrated by portion 204 of hysteresis loop 200 in Figure 4, the anti-parallel to parallel reversal of the magnetization orientation of M_1 in sense layer 122 may be characterized by a sudden change from high resistance to low resistance (i.e., a step transition) as the magnitude of the positive magnetic field is increased. After the magnitude of the applied magnetic field Hx surpasses the critical magnetic field Hc, any further increase in the magnitude of the magnetic field has no effect on the resistance R.

[0030] In one embodiment according to the invention, an electric current is supplied to one or both of write lines 130, 132 to create a magnetic field Hx.

The resistance R of memory cell 120 is measured at a plurality of values of magnetic field Hx, and curves depicting the rate of change of the resistance R with changing magnetic field strength Hx (hereinafter "$\delta R/\delta H$ curves")for the memory cell 120 are determined. The measured $\delta R/\delta H$ curves are compared to model curves as illustrated in Figures 9a and 9b. The model $\delta R/\delta H$ curves of Figures 9a and 9b are derivatives of the hysteresis loop 200 in Figure 4, and reflect the non-symmetrical shape of hysteresis loop 200. Figure 9a shows $\delta R/\delta H$ as the memory cell 120 transitions from an anti-parallel state to a parallel state (portion 204 of hysteresis curve 200), while Figure 9b shows $\delta R/\delta H$ as a memory cell 120 transitions from a parallel state to an anti-parallel state (portion 202 of hysteresis curve 200).

[0031] As can be seen, the model $\delta R/\delta H$ curves of Figures 9a and 9b are significantly different from each other, and can convey more conclusive information about the magnetization orientation of a memory cell than simple resistance measurements. If the measured $\delta R/\delta H$ curve is similar to the model curve shown in Figure 9a, the memory cell 120 is at a high resistance (i.e., anti-parallel) state, and the data stored in the memory cell is a logic value of "1". If the measured $\delta R/\delta H$ curve is similar to the model curve shown in Figure 9b, the memory cell 120 is at a low resistance (i.e., parallel) state, and the data stored in the memory cell is a logic value of "0".

[0032] To obtain complete measured $\delta R/\delta H$ curves, it is necessary to measure resistance R at magnetic field Hx values around the expected critical magnetic field Hc. As discussed above, if the magnitude of Hx exceeds Hc, the measurements will alter the magnetization orientation of memory cell 120 (i.e., destructively read memory cell 120), and thus require that memory cell 120 be rewritten after its magnetization orientation is determined. Such rewriting of the memory cell 120 is not necessarily problematic, except in so far as it requires an additional step in the reading of data from the memory cell. In some instances, however, it is desirable if memory cell 120 is not destructively read, and thus rewriting of memory cell 120 is not required.

[0033] In another embodiment according to the invention, only partial $\delta R/\delta H$ curves are obtained. In particular, resistance R is measured at magnetic field Hx values which are selected to avoid exceeding Hc, such that the magnetization orientation of the memory cell 120 is not altered. As illustrated in Figures 9a and 9b, even for values of Hx that will not alter the magnetization orientation of the memory cell 120, the shape of the $\delta R/\delta H$ curves are different enough from each other to allow comparison of the partial measured $\delta R/\delta H$ curves against the model curves of Figures 9a and 9b.

[0034] Measuring the absolute resistance values of a memory cell to create either complete or partial $\delta R/\delta H$ curves can be difficult, particularly when the change from parallel orientation to anti-parallel orientation or vice versa is not complete (such as along curved portion 202 of hysteresis loop 200 in Figure 4). The ability to determine the magnetization orientation of a memory cell without having to measure absolute resistance values or absolute changes in resistance (as is necessary to determine $\delta R/\delta H$ curves) is desirable.

[0035] In another embodiment according to the invention, the magnetization orientation of memory cell 120 is determined without the need for measuring the absolute resistance values or absolute change in resistance values of the memory cell to create either complete or partial $\delta R/\delta H$ curves, and without risk of altering the magnetization orientation of the memory cell (i.e., a non-destructive read operation). In this embodiment according to the invention, only a relative change in the memory cell resistance R need be observed. Referring to the hysteresis loop 200 of Figure 4, it can be seen that if there is any change in resistance of the memory cell under the application of a magnetic field Hx (either positive or negative) having a magnitude less than the critical magnetic field Hc, then memory cell 120 is in the parallel state. If there is no change in the resistance of memory cell 120, then memory cell 120 is in the anti-parallel state. For example, if memory cell 120 is in the parallel state and a negative magnetic field Hx is applied, a small increase in resistance R will be observed; if a positive magnetic field Hx is applied, no change in resistance R will be observed. If, on the other hand, memory cell 120 is in the anti-parallel state and

a negative magnetic field Hx is applied, no change in resistance R will be observed; similarly, if a positive magnetic field Hx is applied, no change in resistance R will be observed. Thus, the application of only a negative magnetic field Hx allows determination of the magnetization orientation of memory cell 120 based upon the observed change, if any, in resistance R of memory cell 120.

[0036] In one embodiment of the invention, a single conductor (e.g., only one of bit line 132 or word line 130) is energized with an electrical current to create a negative magnetic field Hx around the energized line. The magnitude of the negative magnetic field Hx is kept smaller than the critical magnetic field Hc required to flip the magnetization orientation, so that the magnetization orientation of memory cell 120 is not altered. In one embodiment, the magnitude of Hx is as large as approximately 0.6Hc. As the negative magnetic field Hx is applied, the resistance of memory cell 120 is observed to detect any change in resistance R when the negative magnetic field is applied. As described above, if there is any change in resistance R under the application of a negative magnetic field, then memory cell 120 is in the parallel state. If there is no change in the resistance of memory cell 120, then memory cell 120 is in the anti-parallel state.

[0037] In another embodiment according to the invention, the magnetization orientation of memory cell 120 may be determined when both word line 130 and bit line 132 are energized. This method may be used, for example, when one of the lines 130, 132 is being used to write data to a memory cell 120 different from the memory cell 120 being read. Assuming one of word or bit lines 130, 132 is "on" (i.e., supplied with an electric current), the other line is supplied with an electric current to create a negative magnetic field Hx. As described above, the magnitude of magnetic field Hx is kept smaller than the critical magnetic field Hc necessary to flip the magnetization orientation, so that the magnetization orientation of memory cell 120 is not altered. The resistance of memory cell 120 is observed to detect any resistance change when the negative magnetic field is applied. As described above, if there is any resistance change under the application of a negative magnetic field, then memory cell 120 is in the parallel

state. If there is no resistance change under the application of a negative magnetic field Hx, then memory cell 120 is in the anti-parallel state.

[0038] Whether one or both of write lines 130, 132 are supplied with an electric current to create magnetic fields about the write lines, it is not necessary to know the polarity (positive or negative) of the magnetic field Hx to determine the magnetization orientation of memory cell 120. In one embodiment according to the invention, data may be read (that is, the magnetization orientation may be determined) from a selected memory cell 120 in an array of memory cells by supplying a first current to either one of write lines 130, 132 and creating either a positive or negative magnetic field in the selected write line 130, 132. Memory cell 120 is observed to detect any change in resistance R as the first current is supplied to the selected write line. The first current is then reversed in the selected write line, and memory cell 120 is again observed to detect any change in resistance R as the reversed current is supplied to the selected write line. The magnetization orientation of memory cell 120 may then be determined based on the detected change (if any) in resistance R as the first current and the reversed current are supplied to the selected write line. If no change in resistance R is observed with either the first current or the reversed current, then memory cell 120 is in the anti-parallel state. If a change in resistance R is observed with either the first current or the reversed current, then memory cell 120 is in the parallel state. This same method may also be used if one of write lines 130, 132 is constantly energized, while the other of write lines 130, 132 has its current reversed.

[0039] In each of the embodiments according to the invention, sense layer 122 may be designed or shaped to enhance the edge domain effect described above with respect to Figures 6a-6c and 8a-8c. In particular, sense layer 122 may be created with shapes similar to those described in Figures 10a-10d. The shapes illustrated in Figures 10a-10d effectively change the slope of hysteresis loop as the magnetization orientation changes from parallel to anti-parallel, such that the gradual change in resistance occurs over a greater range of the magnetic field.

[0040] One exemplary system 300 for implementing the various embodiments for reading the magnetization orientation of a memory cell is illustrated in Figure 11. System 300 includes a magnetic memory device 302 having one or more memory cells 120 as described above. Within the magnetic memory device 302, each memory cell 120 is operatively positioned between a conductive word line 130 and a conductive bit line 132. A variable current source 304 is connected to the magnetic memory device 302, such that a current of variable strength and polarity may be independently applied to one or both of the word line 130 and bit line 132 of a selected memory cell 120. The applied current causes a corresponding magnetic field Hx of variable strength and polarity or be applied to selected memory cell 120.

[0041] A resistance measurement module 306 is also connected to the magnetic memory device 302, such that the resistance of the selected memory cell 120 can be observed or measured as the strength and/or polarity of the applied current (and thus the applied magnetic field Hx) is varied. Resistance measurement module 306 may be either software, hardware, or a combination of both, and may be capable of determining relative and/or absolute change in the resistance of selected memory cell 120, depending upon which of the various embodiments for reading the magnetization orientation is being implemented.

[0042] The observed or measured change in resistance of the selected memory cell 120 as a function of the applied magnetic field Hx strength and/or polarity is supplied to a comparator module 308. Comparator module 308 compares the measured or observed behavior of the resistance of memory cell 120 (obtained from resistance measurement module 306) to a model behavior of a memory cell (represented by box 310). Comparator module 308 may be either software, hardware, or a combination of both. The model behavior of memory cell resistance with change as a function of applied magnetic field can be $\delta R/\delta H$ curves as discussed above with reference to Figures 9a and 9b. Alternately, the model behavior of memory cell resistance as a function of applied magnetic field can be a hysteresis loop as discussed above with reference to Figure 4. Based upon comparison of the measured or observed behavior of memory cell 120 to

the model behavior, comparator module 308 determines the status 312 of the magnetic orientation (parallel or anti-parallel) of the selected memory cell 120.